IN THE CLAIMS

1. (Original) A microprocessor including:

a program control unit controlling fetch of an instruction code;

an instruction decode unit decoding said fetched instruction code;

an address operation unit operating an address of a memory on the basis of the result of decoding by said instruction decode unit; and

a data operation unit operating data on the basis of the result of decoding by said instruction decode unit, wherein

said data operation unit executes data transfer between registers and data transfer between said registers and said memory in correspondence to single said instruction code having a single operation code fetched by said program control unit.

2. (Original) The microprocessor according to claim 1, wherein said data operation unit transfers data stored in a first register to said memory and transfers data stored in a second register to said first register in correspondence to a single push instruction fetched by said program control unit.

3. (Original) The microprocessor according to claim 2, wherein said data operation unit decrements the value of a stack pointer after transferring said data stored in said second register to said first register.

4. (Original) The microprocessor according to claim 2, wherein said first register is a work register implemented in said data operation unit.

5. (Original) The microprocessor according to claim 2, wherein said second register is a control register implemented in one of said address operation unit and said program control unit.

6. (Original) The microprocessor according to claim 1, wherein said data operation unit transfers data stored in a first register to a second register and transfers data stored in said memory to said first register in correspondence to a single pop instruction fetched by said program control unit.

7. (Original) The microprocessor according to claim 6, wherein said data operation unit increments the value of a stack pointer after transferring said data stored in said memory to said first register.

8. (Original) The microprocessor according to claim 6, wherein said first register is a work register implemented in said data operation unit.

9. (Original) The microprocessor according to claim 6, wherein said second register is a control register implemented in one of said address operation unit and said program control unit.

10. (Original) The microprocessor according to claim 1, wherein said data operation unit transfers data stored in a first register to said memory and keeps the value of a stack pointer unchanged for a single push instruction fetched by said program control unit.

Claims 11-14 (cancelled)